REMARKS

By this amendment, applicants have added new claims 21-26 to define further aspects of the invention. Claims 21-26 correspond to various ones of claims 4, 10 and 12, but ultimately depend from claim 18.

Claims 1-18 stand rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent Application Publication No. 2001/0026021 A1 to Honda in view of U.S. Patent No. 6,573,739 to Saito. Applicants traverse this rejection and request reconsideration thereof.

The present invention relates to a manufacturing method of a semiconductor integrated circuit device where a burn-in test is performed by causing each of the bumps of a wafer level packaged IC to contact on an electrode surface of a burn-in test socket. After this test is performed, the wafer level packaged IC is removed from the electrode surface of the burn-in test socket by pushing the wafer level packaged IC on "its second metal pad region" with "at least one pushing member" whose contact surface area is narrower than that of the second metal pad region, so as not to cause any damages on "the polymeric resin film." See, Illustrations 4 and 5 attached hereto.

The Honda publication does not relate to a test method, but discloses a recycling method where a wafer level packaged IC is removed from a wiring board by heating the solder bumps over their melting temperature. In this recycling method, Honda employs a metal sheet (30) having bump openings to protect the inner portions of the wafer level packaged IC from heat generated in the bump melting treatments (See Figs. 15a & b).

In other words, the separation between IC and metal terminals on the wiring board in Honda is performed by causing the bumps to melt with heat. As a result, a part of the bumps are pulled off as depicted in Fig. 2B of Honda. In this regard, please note that once largely damaged, bumps will not be used in the very fine wafer level packaged IC. See, the attached Illustration 1.

As the Examiner admits on pages 3 and 4 of the Office Action, the Honda publication neither discloses nor suggests any "second metal pad regions" and "at least one pushing member." From the very beginning, Honda can not be applied to the present manufacturing method because the Honda method relates to a solder (melting and solidification) connection and disconnection technique while the present invention relates to a contact (simply physical contact) connection and disconnection technique.

This Saito patent relates to a test method for a conventional packaged IC (for instance ball grid array) where each of the solder bumps of the IC supported with an IC holder is caused to contact the tip of a contact pin of a test socket (See, the attached Illustration 2).

Since the object of Honda is to provide a flip-chip type semiconductor device which can be recycled, while the Saito patent relates to an IC testing apparatus, it is submitted there would have been no apparent reason to use the teachings in Saito to modify the method disclosed in Honda. Even assuming, arguendo, however, one of ordinary skill in the art would have modified the teachings of Honda based on the teachings of Saito, it is submitted the combined teachings would not have rendered obvious the presently claimed invention for the following reasons.

Saito neither discloses nor suggests any wafer level packaged ICs. Furthermore, Saito neither discloses nor suggests any removing processes. This is

because, as illustrated in the attached Illustration 3, the ball grid array package has a hard and thick outer surface, and there is not a thin and fragile film as the "polymeric resin film (protective film)" as in the present invention. Therefore, Saito does not relate to the presently claimed removing process.

As illustrated in Illustration 6, if the device holder of Saito is applied to the wafer level packaged IC of the present invention, the device holder will cause serious damage to the polymeric resin film and drastically reduce the reliability of the device.

Thus, even assuming, arguendo, one of ordinary skill in the art would have combined the teachings of Honda and Saito, the combined teachings would not have rendered obvious the presently claimed invention including, inter alia, after performing a burn-in test, separating the metal protection electrodes and bumps of the first semiconductor integrated circuit chip from each other by pushing at least one of the plural second metal pad regions on the bump formation surface on such a direction that the first semiconductor integrated circuit chip and the electrode surface go away from each other by bringing at least one pushing member whose contact surface is narrower than the at least one second metal pad region into contact with at least one second metal pad region, as presently claimed.

For the foregoing reasons, it is submitted the presently claimed invention is patentable over the proposed combination of Honda and Saito.

Claims 19 and 20 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Honda et al. in view of Saito and further in view of U.S. Patent No. 6,518,781 to Masuda. Applicants traverse this rejection and request reconsideration thereof.

The Examiner has cited the Masuda patent as allegedly teaching metal protection electrodes formed by forming a plating layer having gold as a main component on a core member having nickel as a main component, wherein each of the metal projection electrodes is formed by further plating, with rhodium, the plating layer having gold as the main component. However, clearly nothing in Masuda remedies any of the basic deficiencies noted above with respect to Honda and Saito. Accordingly, the presently claimed invention is patentable over the proposed combination of documents, at least for the reasons noted above.

In view of the foregoing amendments and remarks, favorable reconsideration and allowance of all of the claims now in the application are requested.

To the extent necessary, applicants petition for an extension of time under 37 CFR 1.136. Please charge any shortage in the fees due in connection with the filing of this paper, including extension of time fees, to the deposit account of Antonelli, Terry, Stout & Kraus, LLP, Deposit Account No. 01-2135 (Case: 045.46647X00), and please credit any excess fees to such deposit account.

Respectfully submitted,

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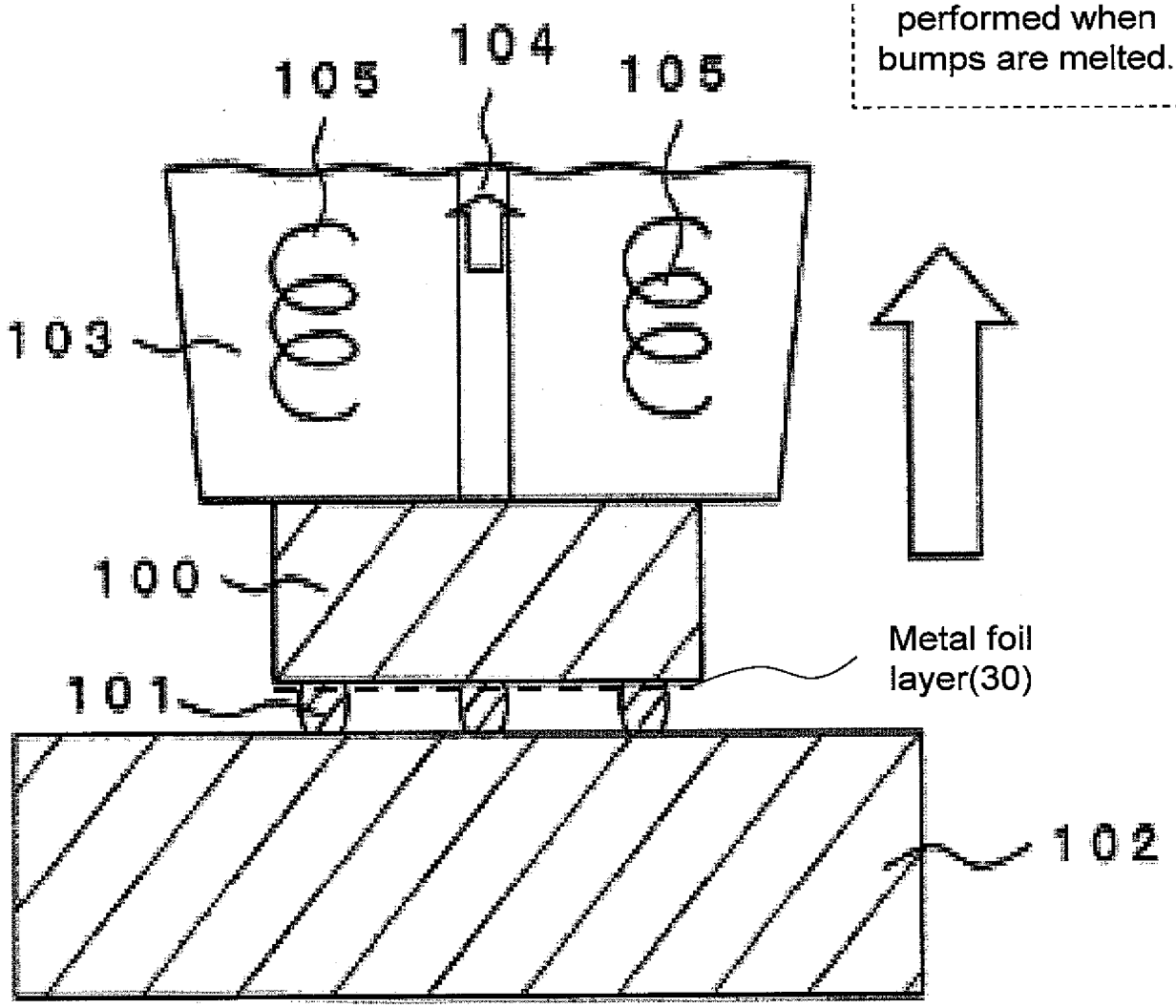
Illustration 1

100: Semiconductor Device
101: Solder Bump
102: Wiring Substrate
103: Heat Absorption Tool
104: Exhaust Pipe
105: Heater

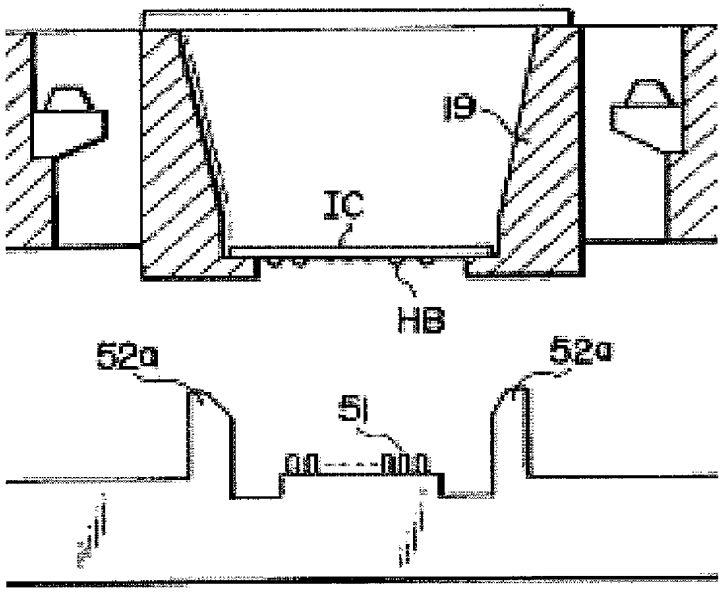
The separation is performed when bumps are melted.



Honda, US 2001/0026021(Fig.2A)

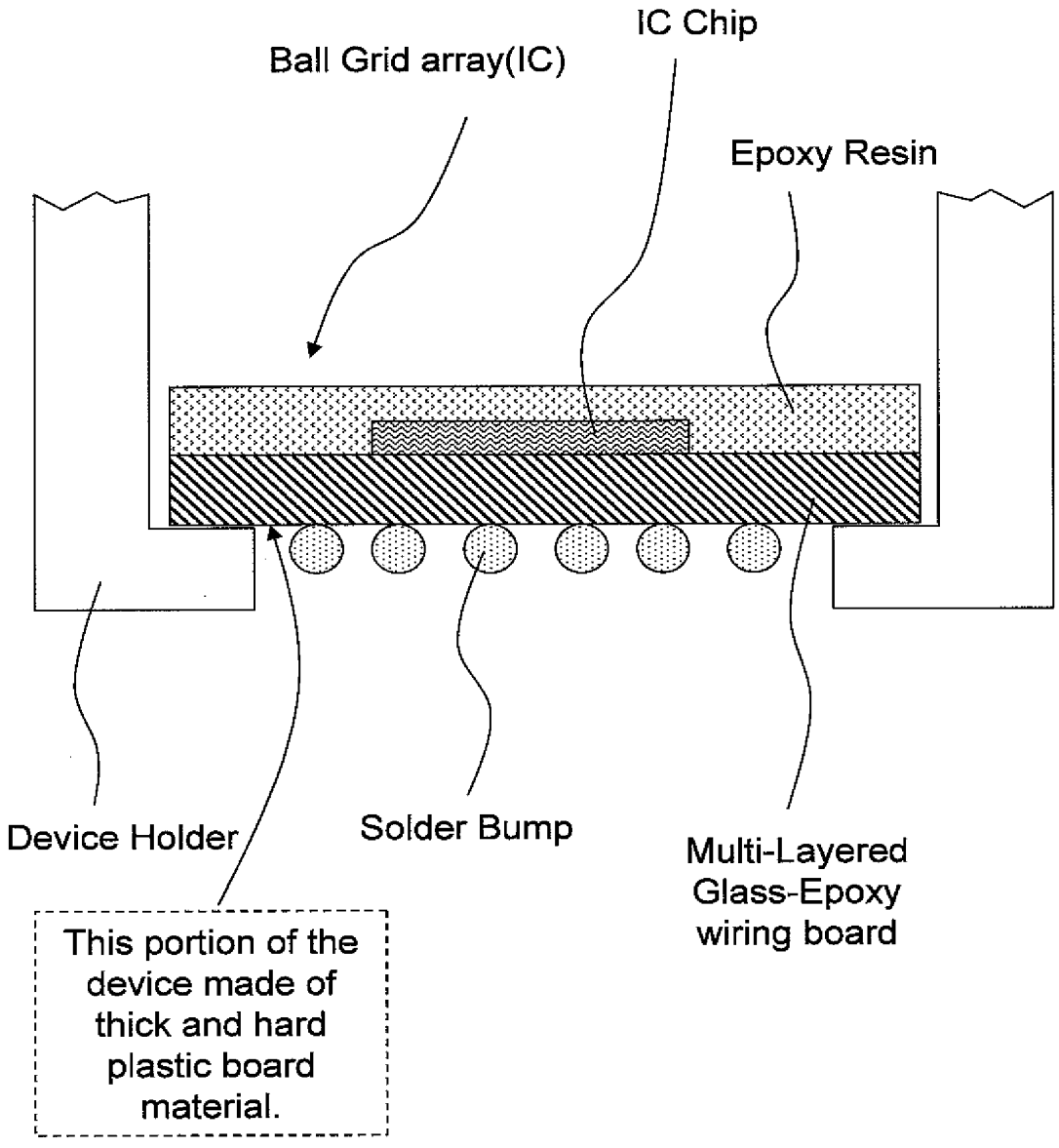
Illustration 2

19: IC holder
51: Contact Pin
52a: Wall of Device Guide
HB: Solder ball
IC: Integrated Circuit device



Saito, USP 6,573,739(Fig.10)

Illustration 3

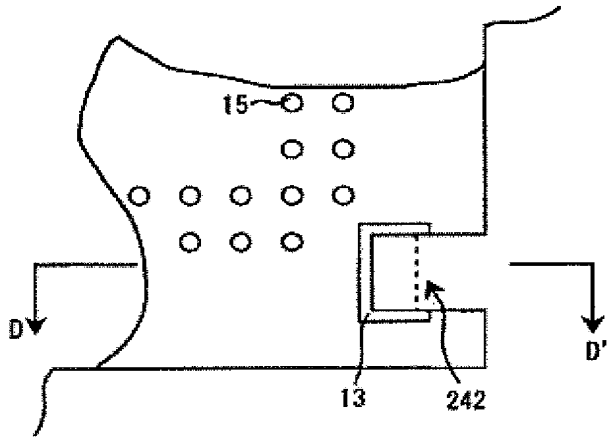


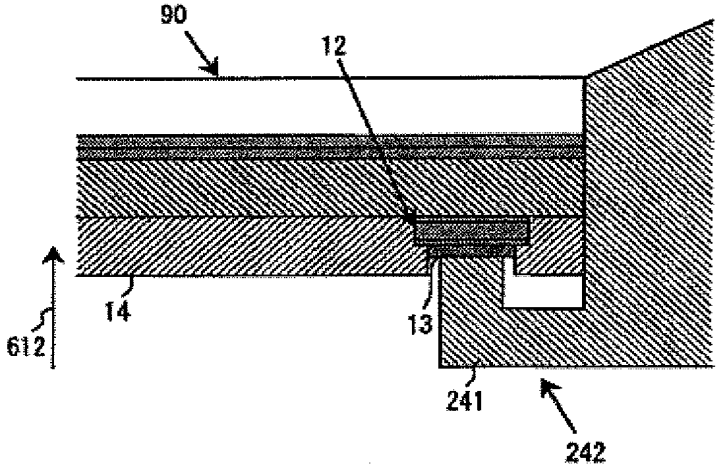
IC in Saito, USP 6,573,739

Illustration 4

12: Re-Wiring Layer
13: Contact Target
14: Protective Film
15: Solder Bump

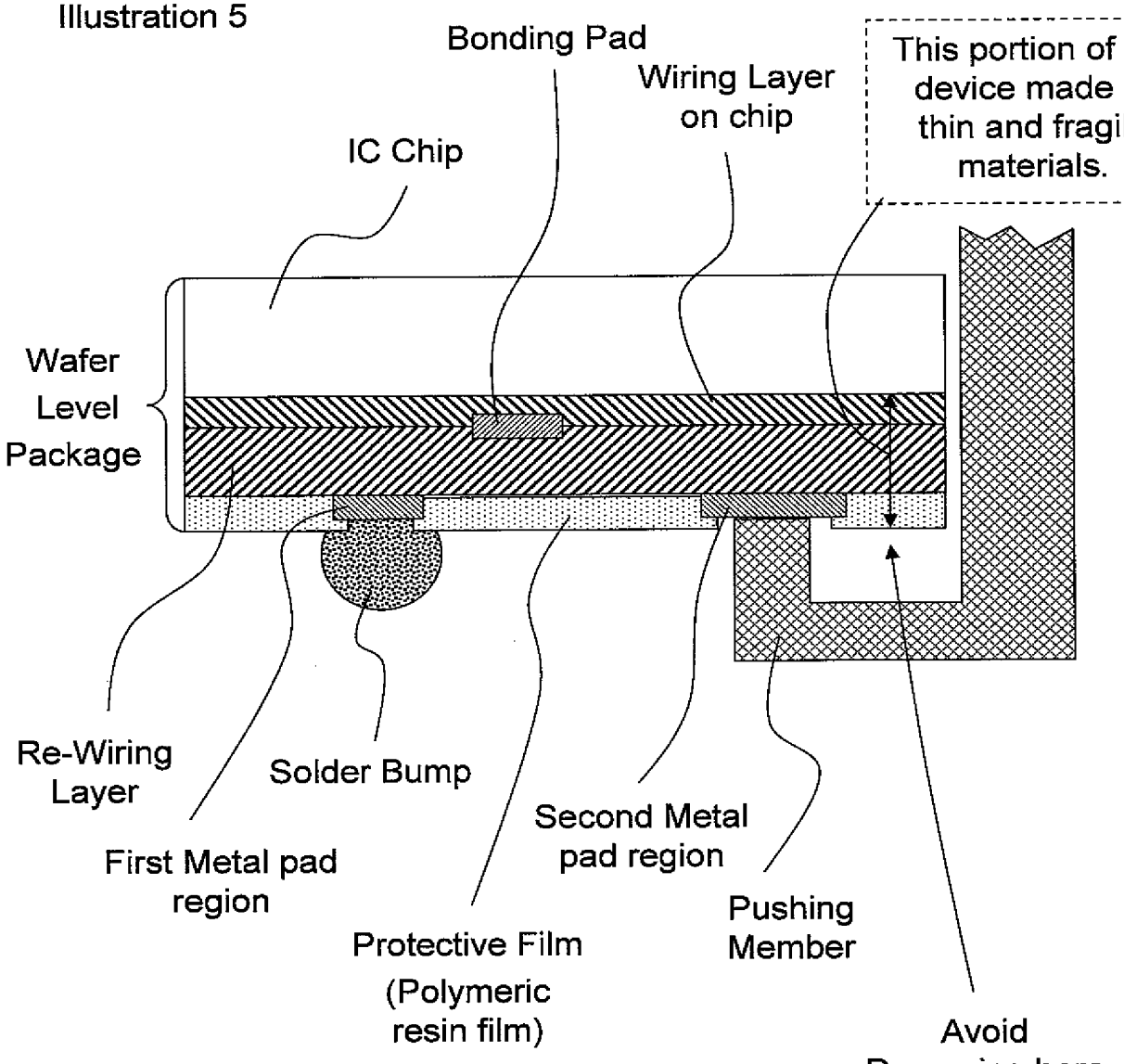
90: Integrated Circuit Device
241: Pushing Member
242: Supporting Arm





MAKIHIRA, et al., USSN 10/594,116(Fig.3B & C)

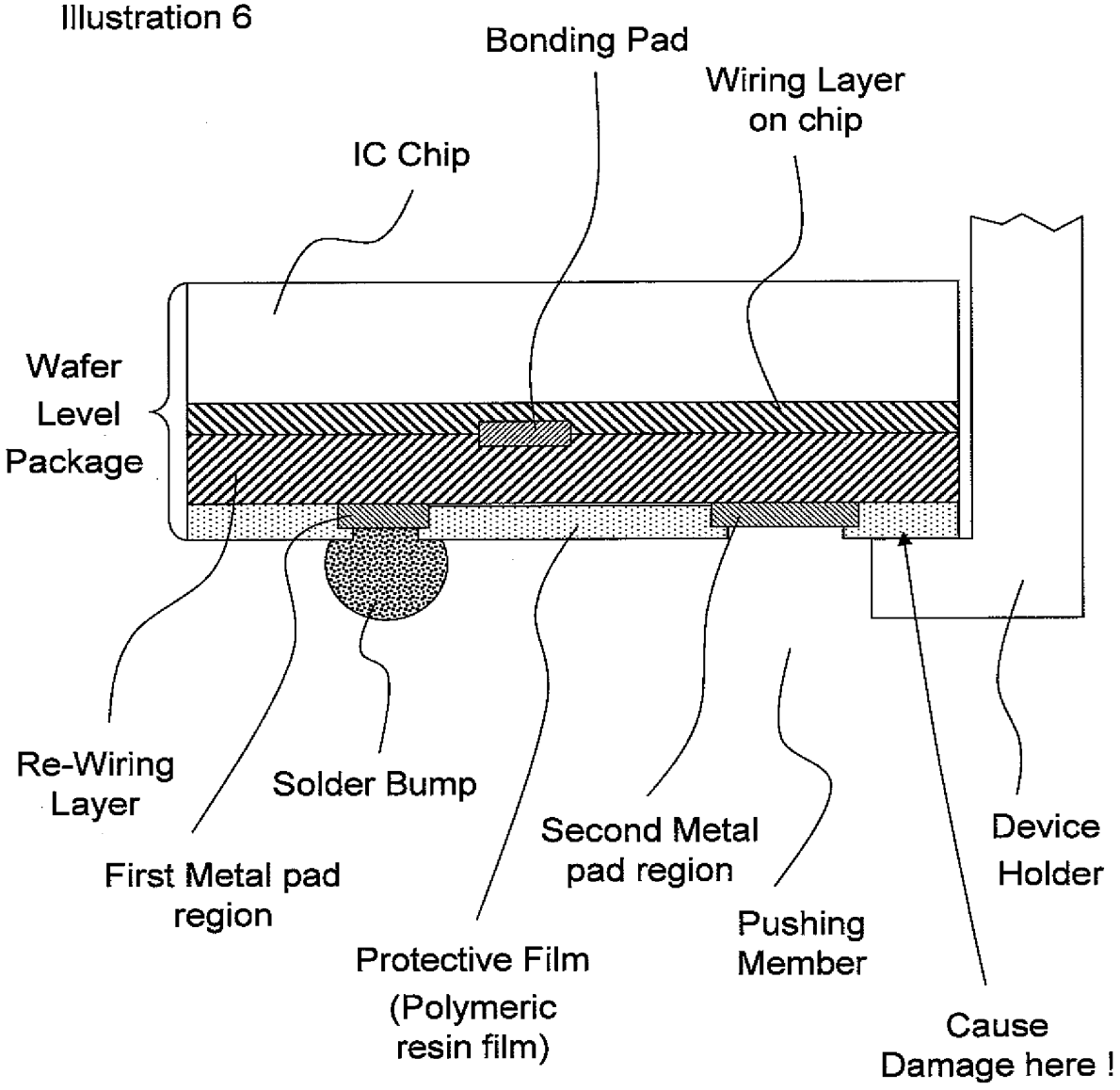
Illustration 5



Enlarged Schematic illustration of Fig.3C and Fig.11 of MAKIHIRA, et al., USSN 10/594,116

Electrical contact and separation between the solder bumps and metal terminals on the wiring board are performed physically at a temperature lower than the melting point of the solder bumps.

Illustration 6



If Saito's Device holder is applied to the wafer level packaged IC of Makihira, What will happen ?